



STANDARDS

Staff Report

October 2025

Japan TC Chapter Meeting

SEMI Global 2025 & 2026 Calendar of Events

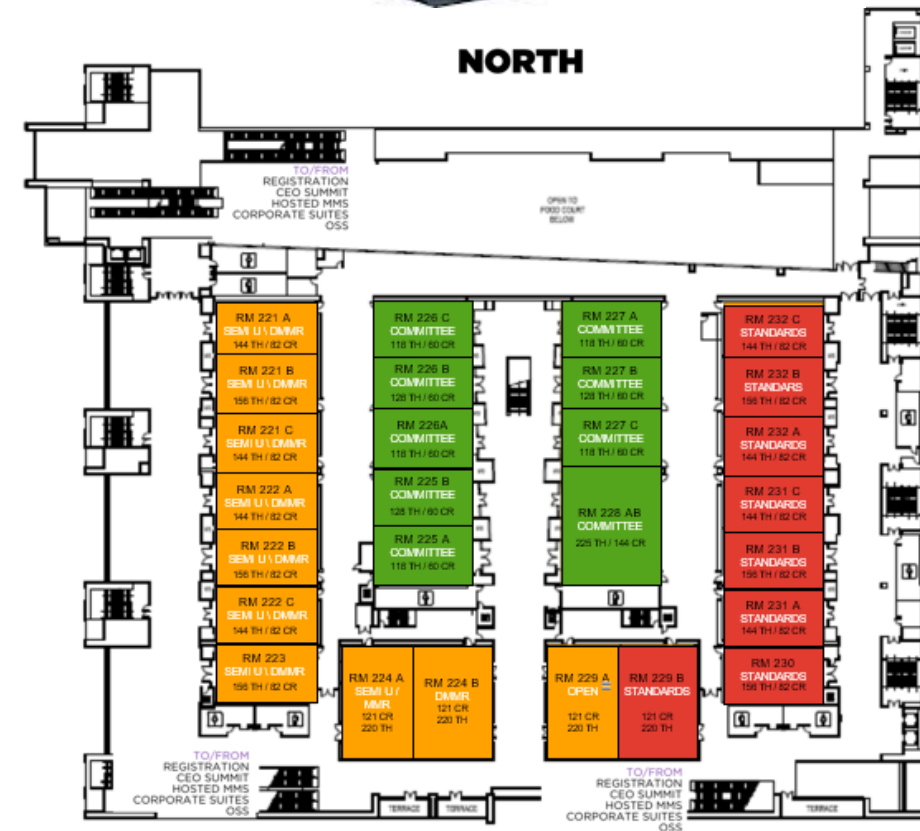
Event Name	Event Details
SEMICON[®] WEST	Oct 07-09, 2025 Phoenix, Arizona
SEMICON[®] EUROPA	Nov 18-21, 2025 Munich, Germany
SEMICON[®] JAPAN	Dec 17-19, 2025 Tokyo, Japan
SEMICON[®] KOREA	Feb 11-13, 2026 Seoul, Korea
SEMICON[®] CHINA	March 25-27, 2026 Shanghai, China
SEMICON[®] SOUTHEAST ASIA	May 05-07, 2026 Kuala Lumpur, Malaysia

SEMICON West 2025-2030

- **2025—October 7-9 | Phoenix Convention Center | Phoenix, AZ**
- 2026—October 13-15 | Moscone Center | San Francisco, CA
- **2027—October 12-14 | Phoenix Convention Center | Phoenix, AZ**
- 2028—October 10-12 | Moscone Center | San Francisco, CA
- **2029—October 9-11 | Phoenix Convention Center | Phoenix, AZ**
- 2030—October 29-31 | Moscone Center | San Francisco, CA

SEMICON West 2025

- **Phoenix Convention Center**
 - 100 North Third Street, PHOENIX, AZ 85004
- **Standards Meetings Location**
 - North Building | 200 Level



SEMI Global Standards Summit (GSS) 2025

@SEMICON West 2025

Date/Time: Tuesday, October 7 | 1:30 PM to 5:30 PM | North Building, 200 Level, Room 229A

Theme: **Future Standards for Connected & Sustainable Semiconductor Manufacturing**

Session Description: The Global Standards Summit is a strategic forum dedicated to identifying standards-critical areas and advancing an industry-wide standardization roadmap for the next 3- and 7-year horizons. Building on the momentum of the inaugural Summit—which spotlighted essential topics such as environmental sustainability—this year’s gathering continues that dialogue while expanding focus to include emerging challenges like supply chain traceability.

With increasing fragmentation across the global microelectronics supply chain driven by geopolitical and other disruptive forces, the need for unified standards is more critical than ever. This Summit provides a timely opportunity to convene, collaborate, and identify the standards that will address these challenges and foster greater industry alignment. We encourage you to join, engage, and help shape the future of standards.

<https://www.semiconwest.org/programs/global-standards-summit>

Global Standards Summit (GSS2025)

@ SEMICON West 2025



Agenda – October 7:

- **(1:30 PM to 1:40 PM)** Welcome & Reminders
- **(1:40 PM to 1:55 PM)** Introduction & Level-setting
- **(1:55 PM to 3:05 PM) Topic 1: Supply Chain Traceability** {Moderator: **Eric Bruce / Samsung**}
 - (1:55 PM to 2:05 PM) Session Intro
 - (2:05 PM to 2:20 PM) Semiconductor Chip Customer Perspective {**Daniel O'Loughlin / Qualcomm**}
 - (2:20 PM to 2:35 PM) Provenance (how to trace all the way up the supply chain) {**Randy Hall / Provenance Chain Network**}
 - (2:35 PM to 2:50 PM) Security (ensuring products are not tampered with or authentic/not counterfeit) {**Neal Edwards / AMD**}
 - (2:50 PM to 3:05 PM) Preventing Supply Chain Disruption {**Krish Dharma / SEMI**}
- **(3:05 PM to 3:15 PM)** Topic 1 Q&A
- **(3:15 PM to 3:25 PM)** Break
- **(3:25 PM to 4:20 PM) Topic 2: Environmental Sustainability** {Moderator: **Joy Marsalla / Lam Research**}
 - (3:25 PM to 3:35 PM) Session Intro
 - (3:35 PM to 3:50 PM) PFAS - Transparency {**Patrick Gottsacker / Intel**}
 - (3:50 PM to 4:05 PM) Energy Efficient Manufacturing {**Slava Libman / FTD solution**}
 - (4:05 PM to 4:20 PM) Environmental Sustainability Considerations in Building Future Facilities {**Nate Monosoff / Jacobs**}
- **(4:20 PM to 4:30 PM) Topic 2 Q&A**
- **(4:30 PM to 5:15 PM) Panel Session** {Moderators: **Supika Mashiro/TEL; Paul Trio / SEMI**}
- **(5:15 PM to 5:30 PM)** Wrap-up & Next Steps
- **(5:30 PM)** Adjourn


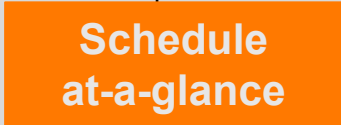
North America Standards Awards & Networking Event

Tuesday, October 7
6:00 PM to 7:30 PM Pacific

Panelists:

- | | |
|-----------------------------|-------------------------------|
| • Eric Bruce / Samsung | • Joy Marsalla / Lam Research |
| • Dan O'Loughlin / Qualcomm | • Patrick Gottsacker / Intel |
| • Randy Hall / PCN | • Slava Libman / FTD solution |
| • Neal Edwards / AMD | • Nata Monosoff / Jacobs |
| • Krish Dharma / SEMI | • Alex Milshteen / Intel |

Standards Meetings @SEMICON West 2025

Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
	6	7	8	9	10	
	EH&S					
	Facilities & Gases			FHE		
	Information & Control					
	Liquid Chemicals					
	MEMS/NEMS			Metrics		
	Physical Interfaces & Carriers					
	Silicon Wafer					
			3D P&I			
						

Upcoming NA Meetings 2026

Previously Reported

Event Name	Date/Venue
NA Winter Meeting	Feb 23-26, 2026 <i>(tentative)</i> SEMI HQ, Milpitas, California/USA
NA Spring Meeting	June 1-4, 2026 <i>(tentative)</i> SEMI HQ, Milpitas, California/USA
SEMICON West Meeting	October 12-15, 2026 San Francisco, California/USA

Upcoming NA Meetings 2026

Proposed

Event Name	Date/Venue
NA Winter Meeting	Feb 23-26, 2026 <i>(tentative)</i> (Full Virtual)?
NA Spring Meeting <i>(In conjunction with ASMC)</i>	May 11-14, 2026 Hilton Albany, New York
SEMICON West Meeting	October 12-15, 2026 San Francisco, California/USA

SEMI Advanced Semiconductor Manufacturing Conference (ASMC)

- About ASMC
 - SEMI's international technical conference for discussing solutions that improve the collective manufacturing expertise of the semiconductor industry.
 - Provides a platform for semiconductor professionals to network and learn the latest in the practical application of advanced manufacturing strategies and methodologies.
- 2025 Venue: May 5-8 | Albany, NY
- 2025 Conference Topics:

<ul style="list-style-type: none"> ➤ Advanced Process Control ➤ Advanced Equipment Process and Materials ➤ Advanced Metrology ➤ Big Data Management and Machine Learning ➤ Contamination Free Manufacturing ➤ Defect Inspection and Reduction ➤ Equipment Optimization 	<ul style="list-style-type: none"> ➤ Factory Automation ➤ High-Volume Manufacturing in the Age of AI ➤ Industrial- and Factory-Automation Design and Manufacturing Sustainability ➤ Novel Devices and Advanced Patterning ➤ Workforce Development ➤ Yield Enhancement / Methodologies
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- ASMC 2026: May 11-14 | Hilton Albany | Albany, NY





ASMC

ADVANCED SEMICONDUCTOR MANUFACTURING CONFERENCE



ASMC

ADVANCED SEMICONDUCTOR MANUFACTURING CONFERENCE

MAY 5-8, 2025 | HILTON ALBANY, ALBANY, NY

WEDNESDAY, MAY 7 CONTINUED

SESSION 13	ADVANCED PROCESS CONTROL 2	SESSION 14	WORKFORCE DEVELOPMENT
4:00	<p>13.1 Arc Detection Algorithm Using Photo Multiplier Tubes S. Kim, M. Kwak, H. Kim, S. Kim, C. Kim, M. Song, J. Lee, J. Park, Y. Kim, Samsung Electronics; J. Park, Tata Electronic</p> <p>13.2 The Utilization of Mathematical Trends to Characterize Equipment Manipulation at Process Temperature for Leveling a CVD Film C. Schweb, R. Boyne, O. Muglikar, Micron Technology</p> <p>13.3 A Novel Multi-Variate Anomaly Detection Method for Chemical Vapor Deposition Y. Khoo, K. Ang, Z. Ooi, GlobalFoundries</p>	<p>4:00</p>	<p>14.1 Curricula, Courses, Labs and Software for Maximum Semiconductor Manufacturing Experience R. Pearson, RIT Microelectronic Engineering; K. Hirschman, P. Mohseni, S. Bolster, Rochester Institute of Technology; J. Tiepelt, FabuSoc; I. Chizmar, Chain Reaction Systems</p> <p>14.2 Developing an Ambidextrous Workforce for Nanoscale Manufacturing C. Weber, J. Yang, Portland State University</p> <p>14.3 SEMI Foundation Special Presentation S. Liss, SEMI</p>
5:05-6:30	<p>PANEL DISCUSSION HIGH VOLUME MANUFACTURING IN THE AGE OF AI Moderator Marie Tripp, Vice President, UNISERS Panelists</p> <ul style="list-style-type: none"> Safa Kutup Kurt, Global Head of Plant Operations and Digital Transformation, EMD Electronic Pawitter Mangat, Vice President, Global Tapeout & Mask Ops, GlobalFoundries Ross Kunz, Data Scientist, Idaho National Laboratory Michael Passow, Senior Technical Staff, IBM Semiconductor Jason Komorowski, Senior Automation and Analytics Engineer, Intel Corporation 	<p>Sponsored by Seeq</p>	

THURSDAY, MAY 8

7:00-8:00am	REGISTRATION & BREAKFAST		
SESSION 15	ADVANCED EQUIPMENT PROCESSES AND MATERIALS 2	SESSION 16	ADVANCED METROLOGY 3
8:00am	<p>15.1 A New and Innovative In-Situ Plasma Etch Pin-Up Clean for Defect Reduction and Process Simplification J. Ye, B. Crandley, G. Song, Micron Technology</p> <p>15.2 Defectivity in Silicon Nitride Etching with Phosphoric Acid in a Single Wafer Processing W. Lo, A. Ramirez, M. Sankarapandian, IBM Research; T. Hinode, M. Packiam, SCREEN SPC USA</p> <p>15.3 Denuded Zone Formation by High Temperature Inert Anneal of 300 mm Cz-Silicon Wafers O. Storbeck, D. Orlov, J. Rittmeyer, A. Kretschmar, A. Klee, L. Palika, K. Gabbard, Infineon Technologies</p> <p>15.4 Void Defect Improvement with Barrier Metal-Cu Seed and Electroplating Recipes Optimization A. Patel, P. Sitterle, J. Martin, Samsung Austin Semiconductor</p>	<p>8:00am</p>	<p>16.1 Contribution of Raman Spectroscopy to Strain Metrology in Trench Array Structures E. Mellet, B. Gergaud, V. Le, GEA Leti; M. Mamoux, LEPHI/INPG, D. Montell, R. Duru, D. Le Curff, C. Le Maout, T. Dalleau, V. Brouzet, STMicroelectronics</p> <p>16.2 Compositional Analysis of Thick Silicon Nitride Films Using X-Ray Photoelectron Spectroscopy S. Kar, L. Carpenter, Y. Timalina, C. Baiocco, D. Harame, AIM Photonics; S. Schujman, NY Creates</p> <p>16.3 Correlation Between In-Situ Wafer-Level Temperature Distribution During the Etch Process and via Resistivity M. Ross, KLA; M. Gerson, G. Renck, E. Mattiavel, STMicroelectronics</p> <p>16.4 Cryogenic Plasma Etching Process Optimization Using a Wireless CryoTemp™ Metrology Wafer H. Zhang, P. Tie, A. Shenai, KLA; A. Alstti, H. Matsusaka, Q. Xu, Lam Research</p>
9:25	COFFEE BREAK	9:25	COFFEE BREAK
SESSION 17	YIELD ENHANCEMENT / YIELD METHODOLOGIES 3	SESSION 18	FACTORY AUTOMATION
9:40am	<p>17.1 Effect of Plasma RF State 0 Pulsing Power on Micro-Loading and Cross-Wafer Uniformity in High Aspect Ratio Contact Etch J. Ye, B. Crandley, V. Subramanian, Y. Jia, C. Tsang, M. Frachel, D. MacMahon, Micron Technology</p> <p>17.2 Characterization of Single Mask MIM Capacitor with Copper Damascene Metallization Y. Peck, J. Xie, Y. Chen, L. Kwok, D. Huang, A. Kumar, M. Islam, C. Chong, GlobalFoundries</p> <p>17.3 Metal Layer Oxide Void Leading to a Reliability Failure S. Takedai, H. Sheng, D. Henke, T. Wu, S. Casey, J. Gardner, S. Lau, C. Chau, Micron Technology</p>	<p>9:40am</p>	<p>18.1 Semiconductor Assembly Test Automation and Standardization Research Association Plans, Goals and Simulation Results S. Radloff, J. Young, J. Rudolph, Intel Corporation</p> <p>18.2 Simulation-Based Evaluation of Idle Vehicle Positioning on Logistics Performance in OHT Systems J. Lee, Y. Jang, Korea Advanced Institute of Science and Technology</p> <p>18.3 An Inherently Explainable Approach for Reinforcement Learning Based Dispatching in Semiconductor Frontend Fabs A. Immodino, R. Stoelckermann, Infineon Technologies</p>
10:45	<p>KEYNOTE MARKET UPDATE Robert Maire, President, Semiconductor Advisors</p>		
11:30	CLOSING REMARKS Co-Chairs: Katie Lutker-Lee, TTCA; Samira Bagheri, EMD Electronics		
1:30-5:30pm	WOMEN IN SEMICONDUCTORS (WIS 2025)		

ASMC 2025 agenda as of 04/15/2025. Subject to change

WELCOME RECEPTION

Monday, May 5
6:00-7:00pm

axcelis

POSTER SESSION/RECEPTION

Tuesday, May 6
5:30-7:30pm

semi

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ASMC MOBILE APP ACCESS



Registered email required to log in.
Proceedings available here at the end of the conference

www.semiamerica.org/asmc25-mobile-app

ADVANCED SEMICONDUCTOR MANUFACTURING CONFERENCE (ASMC)

MONDAY, MAY 5

8:30am-5:30pm **SEMI UNIVERSITY (SEMI U) WORKSHOP**
4:00-7:00pm **REGISTRATION**
6:00-7:00 **WELCOME RECEPTION** Sponsored by **axcelis**

TUESDAY, MAY 6

7:00am **REGISTRATION & BREAKFAST**
8:00 **WELCOME TO ASMC 2025** Joe Stockunas, President, SEMI Americas
OPENING REMARKS Co-Chairs: Katie Lutker-Lee, TTCA; Samira Bagheri, EMD Electronics
SPECIAL PRESENTATION
PRESENTATION OF THE ASMC 2024 BEST PAPER & BEST STUDENT PAPER AWARDS
OPENING KEYNOTE
POWERING AI: RISING TO THE CHALLENGE
Pavel Freundlich, Vice President and Chief Technology Officer, onsemi
9:30 **COFFEE BREAK** Sponsored by **TINFICON**

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CONTINUED

ADVANCED SEMICONDUCTOR MANUFACTURING CONFERENCE (ASMC)

TUESDAY, MAY 6 CONTINUED

SESSION 1	YIELD ENHANCEMENT / YIELD METHODOLOGIES 1	SESSION 2	ADVANCED METROLOGY 1
9:50am	<p>1.1 Session Co-Chairs: Aaron Smith, Texas Instruments; Ishtaq Ahsan, IBM Research; Reshmi Mitra, Samsung Austin Semiconductor</p> <p>1.2 Process Optimizations for GDDR SGRAM in Automotive Applications M. Davis, A. Martin, R. T. Bahadur, V. Kolko, S. Molina, K. Watanabe, B. Yao, G. Wang, G. Sung, Micron Technology</p> <p>1.3 Elimination of 3D NAND Through-Array Contact Shortage on Yield Enhancement Y. Chiu, K. Lu, C. Tsai, H. Lee, N. Lian, T. Yang, K. Chen, C. Lu, Macronix International</p> <p>1.4 Side Base Engineering in HBTs for Improving Breakdown and ICES Leakage Characteristics S. Juyal, J. Chow, M. Chai, GlobalFoundries Singapore</p> <p>1.5 DNN-based Predictive Digital Twin for FHE Manufacturing P. Doerschuk, A. Lal, Cornell University</p> <p>1.6 Inline Defect and Logic and Memory Diagnostic Net Path Overlay Analysis Method H. Liu, E. Green, L. Lo, H. Joshi, J. Cheng, H. Guan, A. Pinto, Intel Corporation</p>	<p>9:50am</p>	<p>2.1 Sponsored by Nova Session Co-Chairs: Dr. Delphine Le Cunff, STMicroelectronics; Igor Turcovets, NOVA Measuring Instruments; Saffi Usmani, EMD Electronics</p> <p>2.2 OCD-Machine Learning Based Metrology for Copper Pad Surface for Hybrid Bonding Integration J. Grassland, STMicroelectronics</p> <p>2.3 DUV-Vis-IR Optical Metrology Enhancements with Machine Learning J. Roberts, A. Ntargas, N. Pallikarakis, K. Florios, n&k Technology; M. Coll, STMicroelectronics</p> <p>2.4 GPU-Accelerated Feature Extraction for Vision AI: Autonomous Image Segmentation and Smart Pattern Recognition for Scalable Real-Time AI Processing with 6.6x Faster Performance and 63% Higher Accuracy K. Ahi, G. Fenger, S. Sriram, S. Wu, Siemens EDA</p> <p>2.5 In-Line Raman Spectroscopy for Semiconductors Strain Engineering and Control Z. Szekeres, P. Bellanger, L. Badesse, B. Bolla, N. Laurent, B. Gombiot, G. Nadeau, A. Pongracz, M. Dallery, R. Petrovski, B. Elie, B. Somogyi, Semtech Semiconductor Physics Laboratory; D. Borge, M. Gallard, J. Hartmann, P. Hauchecorne, V. Le, V. Loup, E. Nolot, J. Sturm, A. Sedri, University Grenoble Alpes; CEA Leti, A.L. Farago, Mediso Medical Imaging Systems</p>

11:35 NETWORKING LUNCH

SESSION 3 ADVANCED PROCESS CONTROL 1

1:15pm	<p>3.1 Session Co-Chairs: Agnes Roussy, Mines St Etienne; Daniele Pagano, STMicroelectronics; Raymond Van Roijen, onsemi</p> <p>3.2 Using Machine Vision for Fault Detection of Dry Resist Top Film Peeling R. Good, C. Wan, T. Krauss, J. Pauller, R. Maxwell, GlobalFoundries</p> <p>3.3 Implementation & Application of Coherent Control Systems: Digital Twin (High Frequency Open Loop) with Run-to-Run (Low Frequency Closed Loop) P. Klotz, R. Sarang, H. Allen, S. Drandapani, Applied Materials</p> <p>3.4 A Study on Bare Endpoint Profile Transformation Caused by Different Metal/Via Reticule Transmission Ratio in Oxide Trench Etch Processes D. Huang, S. Mediwara, GlobalFoundries Singapore</p> <p>3.5 IP-Aware Federated Manufacturing Intelligence: Enabling Secure and Collaborative Semiconductor Manufacturing L. Garcia, S. Rini, NYCU; S. Chang, Lam Research; Y. Hsu, National Taipei University of Technology</p>
2:40	COFFEE BREAK

SESSION 5 CONTAMINATION FREE MANUFACTURING

3:00	<p>5.1 Session Co-Chairs: Chris Ebert, Linde, Christopher Long, IBM Research; Jennifer Bragg, Siddarth Sampath, Entegris</p> <p>5.2 A New Continuous Plasma Process for Defect Reduction J. Ye, D. Egbeyemi, A. Fang, W. Simpson, Micron Technology</p> <p>5.3 Yield Loss Due to the Interaction Between Dissolved Oxygen in DI Water and Magnesium in Final Rinse Process A. Dinwashed, Z. Yiwen, T. Sean, L. San, GlobalFoundries</p> <p>5.4 Particle Control for Low-Energy Boron Implantation P. Geisbuhler, D. Burner, C. Free, K. Wenzel, L. Kim, O. Kim, B. Son, Axcelis Technologies; H. Cha, S. Na, SK hynix</p> <p>5.5 Investigation of the Radially Spreading Micro-Bubble Defect Due to Contamination from SEM J. Jeong, E. Ko, Y. Kim, Samsung Electronics</p>
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4:30 TUTORIAL

MATERIALS INTELLIGENCE: ENABLING THE FUTURE OF TECHNOLOGY
Lu Gan, Senior Director, Head of Technology Strategy and Roadmap, EMD Electronics

5:30-7:30 POSTER SESSION / RECEPTION

Scan the QR Code for Poster Session Information



WEDNESDAY, MAY 7

7:00-8:00am	REGISTRATION & BREAKFAST
8:00	KEYNOTE STRATEGIC DIRECTIONS FOR ELECTRONICS PACKAGING Subramanian S. Iyer, Director, UCLA CHIPS—Distinguished
8:45	COFFEE BREAK

SESSION 7A ADVANCED EQUIPMENT PROCESSES AND MATERIALS 1

9:05am	<p>7.1 Session Co-Chairs: Olaf Storbeck, Infineon Technologies; Shrawan Matham, IBM Research; Thirumalesh Bannuru, Wolfpack</p> <p>7.2 Effect of In-Situ Native Oxide Clean on Point Defect Behavior in Si-Amorphized Ion-Implanted Si A. Rivera, K. Jones, University of Florida; N. Kennedy, C. Hatem, Applied Materials</p> <p>7.3 Optimization Epitaxy Process to Reduce Hotspot Problem K. Cheng, Y. Li, J. Huang, GlobalFoundries Singapore; W. Lew, NanYang Technological University</p> <p>7.4 Purification by Paradigm Process Matching: Copy Exact Process or Copy Exact Output? A. Isaacs, B. Isaacs, T. Budri, B. Wofford, G. Neer, R. Smith, Texas Instruments</p>
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SESSION 7B DEFECT INSPECTION AND REDUCTION

10:05	<p>7.1 Session Co-Chairs: Alena Greer, KLA; Srividya Jayaram, Siemens EDA; Shrawan Matha, IBM Research</p> <p>7.2 Full Wafer Inspection for Voltage Contrast Systematic Defects Using High-Throughput Point Scan O. Patterson, Intel Corporation</p> <p>7.3 Accelerated Defectivity Monitoring in High-Volume Manufacturing via Unsupervised AI Techniques H. Overland, M. Pasqualini, A. Girmaud, G. Cui, C. Regnier, STMicroelectronics; V. Ramakrishna, S. Anurag, S. Tummalaipati, A. Tiwari, P. Deevanapati, B. Ries, A. Menon, D. Anas, P. Sharma, P. Paris, H. Kopel, KLA</p> <p>7.4 AI-Powered Anomaly Detection: A Robust, Pattern-Agnostic Faster R-CNN with Scalable GPU-Accelerated Deep Learning for High-Fidelity Computer Vision Defect Identification (mAP: 79%, mAR: 77%, F1: 74.5%) H. Hatan, A. Eidesvik, A. Essam, G. Fenger, K. Ahi, N. Greenelch, H. Samir, S. Jayaram, W. Stewart, Siemens EDA</p>
11:10	<p>BOXED LUNCH & ROBOTICS DEMONSTRATION</p> <p>Sponsored by ERM</p>

SESSION 9 YIELD ENHANCEMENT / YIELD METHODOLOGIES 2

12:50pm	<p>9.1 Session Co-Chairs: Jeff Ye, Micron Technology; Shrawan Matham, IBM Research; Vijayalakshmi Seshachalam, GlobalFoundries</p> <p>9.2 Influence of Salicide Block Oxide and Key Process Parameters on P+ Polysilicon Resistor Performance A. Dinwashed, C. Choi, L. Nam, K. Lau, X. Jin, C. Conne, GlobalFoundries</p> <p>9.3 Enhanced Annealing and Material with Crystal Originated Particles for Localized Yield Improvement K. Cheng, J. Zhou, J. Huang, GlobalFoundries Singapore; W. Lew, NanYang Technological University</p> <p>9.4 Effect of Deposition Conditions on Polysilicon PNP Emitter Grain and Electrical Performance M. Lakshminarayanan, A. Dinwashed, H. Hiew, GlobalFoundries</p>
1:55	COFFEE BREAK

SESSION 11 EO: EQUIPMENT OPTIMIZATION

2:15	<p>Sponsored by Trelleborg</p> <p>11.1 Session Co-Chairs: Olaf Storbeck, Infineon Technologies; Thirumalesh Bannuru, Wolfpack; Vijayalakshmi Seshachalam, GlobalFoundries</p> <p>11.2 Copper Residue Removal from Electrostatic Chuck to Mitigate Helium Leak Faults Using Enhanced In-Situ Chamber Clean R. Thiruchelvan, B. Cheong, W. Wong, GlobalFoundries</p> <p>11.3 Predicting Seal Longevity: Advanced Simulations for Plasma and Rotary Applications in Semiconductor Processes M. Gulcur, J. Palford, T. Duran, F. Dum, A. Asbury, Trelleborg Sealing Solutions</p> <p>11.4 Enhancing Particle Performance in Plasma-Resist-Stripping Machines through Pressure Relief Valve Assembly Relocation R. Goczi, M. Ten, R. Thiruchelvan, C. Foo, GlobalFoundries</p> <p>11.5 CPEC Clean Enhancement via Backside Polishing to Reduce Precoat UPC Fault Z. Ooi, C. Tan, C. Lim, W. Pascoa, B. Tan, C. Koh, GlobalFoundries</p>
3:40	COFFEE BREAK

SESSION 8 SMART MANUFACTURING

9:05am	<p>8.1 Session Co-Chairs: Doug Suerich, PEER Group; Robert Pearson, RIT Microelectronic Engineering; Stefan Radloff, Intel Corporation</p> <p>8.2 From Variations to Precision: Modeling and Optimization of Inner Spacer Etch in GAA FETs P. Kumar, S. Bana, Applied Materials; O. Maheshwari, N. Mohapatra, Indian Institute of Technology Gandhinagar</p> <p>8.3 Improving Machine Calibration Performance Through Systematic Feature Design in Semiconductor Manufacturing M. Sumiya, Y. Kamaj, S. Matsudaira, Hitachi High-Tech; W. Li, University of Cincinnati; D. Ji, J. Lee, University of Maryland, College Park</p> <p>8.4 AI-Powered Etching Architecture Refinement from Small Data in 3D NAND Development C. Tsai, Z. Yang, M. Huang, M. Wu, K. Lu, H. Lee, N. Lian, T. Yang, K. Chen, C. Lu, Macronix International</p> <p>8.5 General Framework for Processing Time Prediction and Machine Availability for All Fab Equipment T. Korabi, G. Goossens, A. Kaushik, J. van Heugten, J. Bedorf, minds.ai; S. Chakraborty, D. Palati, J. Thomas, S. Ramakrishnan, J. Delong, T. Hewlett, GlobalFoundries</p>
11:10	<p>BOXED LUNCH & ROBOTICS DEMONSTRATION</p> <p>Sponsored by ERM</p>

SESSION 10 ADVANCED METROLOGY 2

12:50pm	<p>10.1 Session Co-Chairs: Cody Murray, IBM Research; Delphine Le Cunff, STMicroelectronics</p> <p>10.2 Epi Defect Quantification via Massive Metrology SEM Measurement-Based Inspection C. Smith, F. Levitov, Applied Materials; S. Matham, S. Emans, R. Sheraw, IBM Research</p> <p>10.3 Novel Placement of Overlay Marks to Eliminate Measurement Errors for Thick Photoresist Layers A. Viswanathan, D. Oon, S. Lim, J. Zhou, J. Chew, GlobalFoundries</p> <p>10.4 Orthogonal Marker Structures for Precise Electron Probe Positioning and Displacement Measurement in Secondary Electron Imaging K. Matsuda, S. Leong, Hunan University</p>
1:55	COFFEE BREAK

SESSION 12 NOVEL DEVICES AND ADVANCED PATTERNING

2:15	<p>12.1 Session Co-Chairs: Eric Eisenbraun, SUNY Albany CNSE; Shubhdeep Goswami, GE Aerospace Research; Susan Fan, IBM Research</p> <p>12.2 A Perspective on Interconnect Scaling Challenges in the NanoStack Transistor Era N. Lenakis, S. Khan, J. Mazzeo, U. Bajpai, K. Motoyama, IBM Research</p> <p>12.3 Device Optimization to Enable Ultra Low Leakage Logic FinFETs E. Yamoghaddam, S. Saudari, W. Ma, M. Luque, V. Rossi, A. Orshani, J. Johnson, O. Kwon, E. Maciejewski, H. Wang, S. Parthar, GlobalFoundries</p> <p>12.4 Toward ML-Enhanced Design and Fabrication of Resonant Nanoelectromechanical IR Sensor E. Altin, H. Yan, A. Vardetti, W. Gubini, P. Simeoni, M. Rinaldi, B. Davaji, Northeastern University</p> <p>12.5 WEE Residue Elimination for Cross-Link Prone Positive Tone DUV Photoresist S. Lim, A. Viswanathan, H. Liu, V. Xavier, GlobalFoundries</p>
3:40	COFFEE BREAK

CONTINUED

Critical Dates for SEMI Standards Ballots – 2025

2025	Ballot Submission Deadline	Voting Opens	Voting Closes
Cycle 8	September 3	September 24	October 24
Cycle 9	October 14	October 29	November 28

<https://www.semi.org/en/collaborate/standards/ballots>

Critical Dates for SEMI Standards Ballots 2026

2026	Ballot Submission Deadline	Voting Opens	Voting Closes
Cycle 1	December 16, 2025	January 7	February 6
Cycle 2	January 23	February 11	March 13
Cycle 3	March 5	March 18	April 17
Cycle 4	March 30	April 14	May 14
Cycle 5	May 8	May 27	June 26
...

<https://www.semi.org/en/collaborate/standards/ballots>

SEMI Standards Publications

- Total SEMI Standards in portfolio: 1,107
 - Includes 373 Inactive Standards

Cycle	New	Revised	Reapproved	Withdrawn
May 2025	0	5	4	0
June 2025	1	0	0	0
July 2025	1	4	0	0
August 2025	0	1	0	0
September 2025	4	1	3	0

SEMI Standards Publications

- New Standards

Cycle	Designation	Title	Committee	Region
June 2025	SEMI M94	Specification for Silicon Carbide Engineered Substrates	Compound Semiconductor Materials	EU
July 2025	SEMI E194	Guide to Using a Liquid Particle Counter to Assess Particulate Surface Contamination on Critical Chamber Components and Coupons	Metrics	NA
September 2025	SEMI E195	Test Method Using Adhesive Replacement Substrates to Assess Particulate Surface Contamination on Critical Chamber Components	Metrics	NA
September 2025	SEMI E196	Guide for Equipment Edge Data Governance	Information & Control	TW

SEMI Standards Publications

- New Standards

Cycle	Designation	Title	Committee	Region
September 2025	SEMI M95	Test Method for Net Carrier Density and Resistivity of Silicon Epitaxial Layer by Capacitance-Voltage Measurements with an Evaporated Metal Schottky Diode	Silicon Wafer	JP
September 2025	SEMI T26	Specification for Electronic Supply Chain Traceability Using Distributed Ledger Technology	Traceability	NA

Regulations & Procedure Manual

Available at www.semi.org/standards (under Tools for Developing Standards) or direct link below

- Regulations (Feb 20, 2024)
 - <https://www.semi.org/sites/semi.org/files/2024-02/Standards%20Regulations%20February%2020%202024.pdf>
- Procedure Manual (July 7, 2025)
 - <https://www.semi.org/sites/semi.org/files/2025-07/Procedure%20Manual%20July%2007%2C%202025%20v1.pdf>
 - Noticeable updates:
 - Major revision to multiple Standards
 - New SNARF Form (July 2025)
 - Ballot checklist requirement for Revision to Primary Standard

SEMICON® JAPAN 2025 開催概要 Overview

Period: December 17-19, 2025

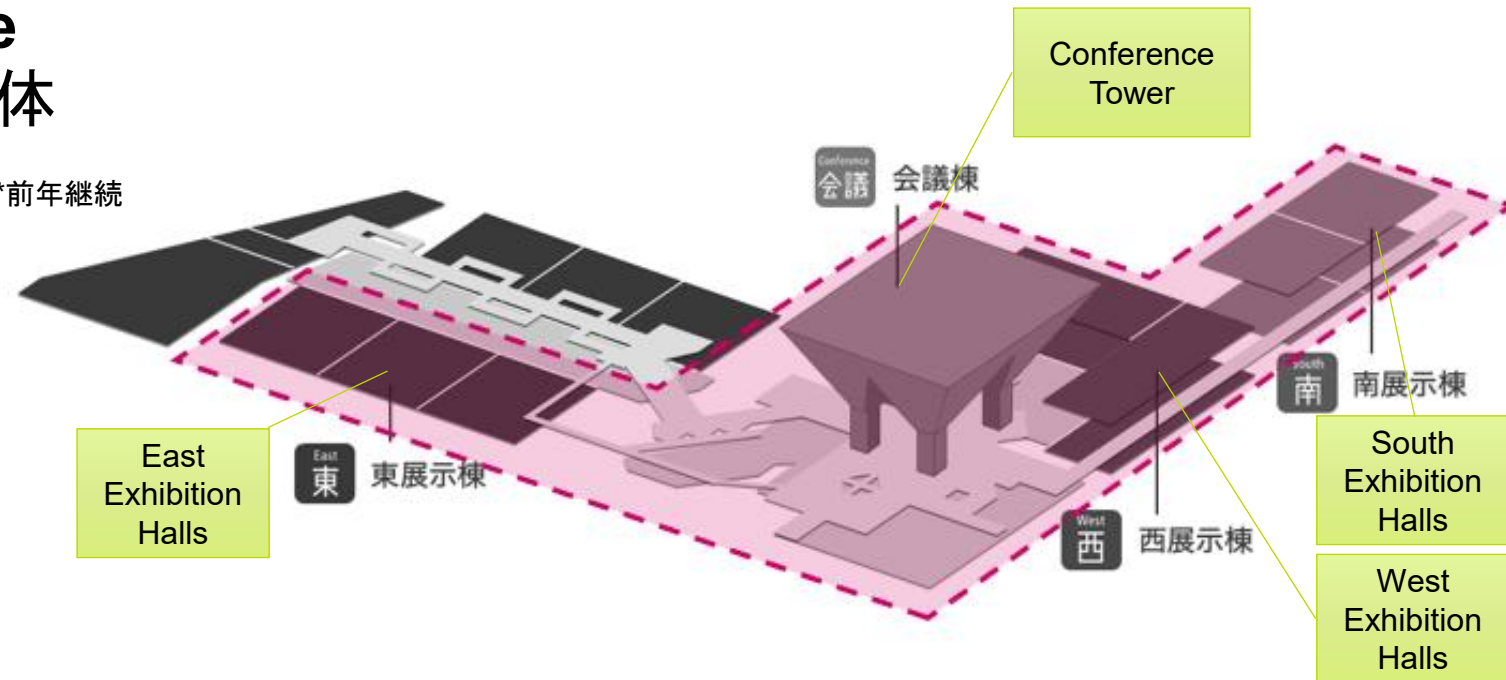
Venue: Tokyo Big Sight, Tokyo, Japan

Organizer: SEMI

SEMICON Japan 2025 Theme

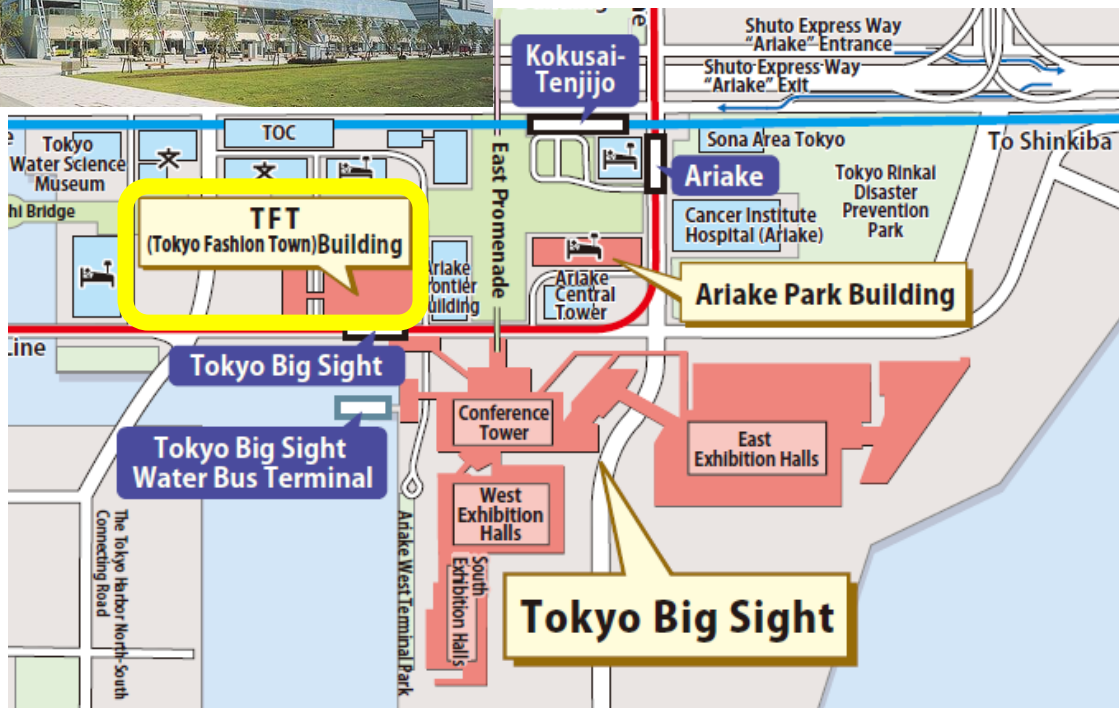
日本語: AI x サステナビリティ x 半導体

英語: STRONGER TOGETHER *前年継続



SEMICON Japan 2025 Standards Meeting

Standards Meetings will be held
at TFT Building
(Not Tokyo Big Site)



TFTビル 東館9F



SJ25: SEMI Standards Meetings

- SEMI Standards will host the below Technical Committees + many Task Forces engaged in various standardization activities and topics, including:
 - Compound Semiconductor Materials
 - Information & Control
 - Metrics
 - Physical Interfaces & Carriers
 - Silicon Wafer
 - Traceability
- SEMI STANDARDS + AWARDS CEREMONY NETWORKING EVENT will be held on Thursday, December 18, 2025, 17:00-19:00.
- Full schedule will be posted on the SEMICON Japan Website soon.
 - [SEMI International Standards | SEMICON Japan](#)

SEMI University Japan Store Launched in June, 2024



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Semiconductor Manufacturing Process – Back-end



Various Semiconductors



Regulatory



SEMI Standards



Check more details at:

<https://store-jp.semi.org/collections/semi-university>

Staff Assignment

Hirofumi Kanno

Senior Manager

JRSC

81.3.3222.6018

hkanno@semi.org

Akiko Yoshida

Senior Coordinator

3D Packaging & Integration,

Compound Semiconductor

Materials, EHS, Gases & Facilities,

Silicon Wafer

81.3.3222.6018

ayoshida@semi.org

Takeaki Hirabara

Coordinator

Information & Control, Liquid
Chemicals, Physical Interfaces &
Carriers

81.3.3222.6018

thirabara@semi.org

Nahoko Koga

Coordinator

Automation Technology, Flexible
Hybrid Electronics, FPD Materials
& Components, FPD Metrology,
Metrics, Traceability

81.3.3222.6018

nkoga@semi.org



THANK YOU

STANDARDS